WHAT IS CLAIMED IS:

1. A single instruction, multiple data (SIMD) controller for processing a plurality of data streams in a digital subscriber line (DSL) system, comprising:

a plurality of circular buffer circuits coupled to store data from said plurality of data streams;

a plurality of address generation circuits coupled to access said data stored in said plurality of circular buffer circuits;

a plurality of processor circuits coupled to process said data accessed by said plurality of address generation circuits; and

a program control unit coupled to control said plurality of processor circuits with an instruction.

2. The controller of claim 1, wherein one of said plurality of circular buffer circuits comprises:

a first section coupled to store one or more symbols before being processed;

a second section coupled to store said one or more symbols being processed; and

a third section coupled to store said one or more symbols after being processed.

3. The controller of claim 1, wherein one of said plurality of address generation circuits comprises:

a symbol manager circuit coupled to generate an input base address, a processor base address, and an output base address,

wherein said one of said plurality of address generation circuits is further coupled to receive an input offset address, a processor offset address, and an output offset address, and to generate an input address, a processor address, and an output address in accordance with said input base address, said processor base address, and said output base address.

4. The controller of claim 1, wherein said plurality of processor circuits are further coupled to receive a plurality of enable signals and to selectively process said data based on said plurality of enable signals.

5. The controller of claim 1, wherein said plurality of address generation circuits are further coupled to selectively generate a plurality of enable signals, depending upon whether a full symbol is ready for processing in each of said plurality of address generation circuits.

6. The controller of claim 5, wherein said plurality of processor circuits are further coupled to receive said plurality of enable signals and to selectively process said data based on said plurality of enable signals.

7. The controller of claim 1, wherein said plurality of address generation circuits are further coupled to selectively generate a plurality of enable signals, depending upon a difference between an input base address and a processor base address in each of said plurality of address generation circuits.

8. A method of processing a plurality of data streams in a digital subscriber line (DSL) system, comprising the acts of:

calculating a plurality of input addresses for said plurality of data streams based on a plurality of input base addresses and a plurality of input offset addresses;

storing a plurality of data from said plurality of data streams according to said plurality of input addresses;

calculating a plurality of processor addresses for the stored plurality of data based on a plurality of processor base addresses and a plurality of processor offset addresses;

processing, using a single instruction, the stored plurality of data according to said plurality of processor addresses;

calculating a plurality of output addresses for the processed plurality of data based on a plurality of output base addresses and a plurality of output offset addresses;

outputting the processed plurality of data according to said plurality of output addresses; and

updating said plurality of input base addresses, said plurality of processor base addresses, and said plurality of output base addresses.